

What is claimed is:

1 1. A method comprising:

2 partitioning a memory device to produce a first
3 group of memory entries being accessible in parallel and
4 selectable independent of a second group of memory
5 entries in the memory device that is accessible in
6 parallel.

1 2. The method of claim 1, further comprising:

2 partitioning a memory entry in the first group of
3 memory entries into sub-entries.

1 3. The method of claim 1, further comprising:

2 selecting the first group of memory entries for
3 accessing in parallel.

1 4. The method of claim 1 wherein the memory device is
2 included in a multithreaded engine of a packet processor.

1 5. The method of claim 1 wherein the first group of memory
2 entries store a first type of data and the second group of
3 memory entries store a second type of data.

1 6. The method of claim 2 wherein the memory entry includes
2 at least two subentries.

1 7. The method of claim 2 wherein the memory entry includes a
2 combination of subentries.

1 8. A computer program product, tangibly embodied in an
2 information carrier, the computer program product being
3 operable to cause a machine to:

4 partition a memory device to produce a first group
5 of memory entries being accessible in parallel and
6 selectable independent of a second group of memory
7 entries in the memory device that is accessible in
8 parallel.

1 9. The computer program product of claim 8 being further
2 operable to cause a machine to:

3 partition a memory entry in the first group of
4 memory entries into sub-entries.

1 10. The computer program product of claim 8 being further
2 operable to cause a machine to:

3 select the first group of memory entries for
4 accessing in parallel.

1 11. A computer program product of claim 8 wherein the memory
2 device is included in a multithreaded engine of a packet
3 processor.

1 12. The computer program product of claim 8 wherein the first
2 group of memory entries store a first type of data and the
3 second group of memory entries store a second type of data.

1 13. The computer program product of claim 9 wherein the
2 memory entry includes at least two subentries.

1 14. The computer program product of claim 9 wherein the
2 memory entry includes a combination of subentries.

1 15. A content-addressable memory (CAM) manager comprises:
2 a process to partition a memory device to produce a
3 first group of memory entries being accessible in
4 parallel and selectable independent of a second group of
5 memory entries in the memory device that is accessible in
6 parallel.

1 16. The CAM manager of claim 15 further comprising:
2 a process to partition a memory entry in the first
3 group of memory entries into sub-entries.

1 17. The CAM manager of claim 15 further comprising:
2 a process to select the first group of memory
3 entries for accessing in parallel.

1 18. A system comprising:

2 a memory device capable of being partitioned to
3 produce a first group of memory entries that is
4 accessible in parallel and selectable independent of a
5 second group of memory entries in the memory device that
6 is accessible in parallel.

1 19. The system of claim 18 wherein a memory entry in the
2 first group of memory entries is capable of being partitioned
3 into sub-entries.

1 20. The system of claim 18 wherein the first group of memory
2 entries is further capable of being selected for accessing in
3 parallel.

1 21. A packet forwarding device comprising:

2 an input port for receiving a packet;
3 and output port for delivering the received packet;
4 and

5 a memory device capable of being partitioned to
6 produce a first group of memory entries that is
7 accessible in parallel and selectable independent of a
8 second group of memory entries in the memory device that
9 is accessible in parallel.

1 22. The packet forwarding device of claim 21 wherein a memory
2 entry in the first group of memory entries is capable of being
3 partitioned into sub-entries.

1 23. The packet forwarding device of claim 21 wherein the
2 first group of memory entries is further capable of being
3 selected for accessing in parallel.

1 24. A content-addressable memory (CAM) comprising:
2 a first group of memory entries being accessible in
3 parallel and selectable independent of a second group of
4 memory entries in the CAM that is accessible in parallel.

1 25. The CAM of claim 24 wherein a memory entry in the first
2 group of memory entries is capable of being partitioned into
3 sub-entries.

1 26. The CAM of claim 24 wherein the first group of memory
2 entries is further capable of being selected for accessing in
3 parallel.